

## WHAT IS CLAIMED IS:

## 1. A clock and data recovery circuit comprising:

a plural number of latch circuits, receiving an input data in common, for sampling the input data with transition edges of clocks having phases shifted from one another, said clocks supplied respectively  
 5 to said latch circuits, and for outputting the sampled data;

a phase detection circuit for detecting a phase of a transition point of said input data associated with the clocks from outputs of said plural latch circuits and for outputting the detected phase;

a filter for smoothing an output of said phase detection circuit; and

10 a circuit for controlling the phase of said clocks based on an output of said filter; said clock and data recovery circuit recovering the clocks and data based on the input data; wherein

a circuit for supplying the clocks with phases shifted from one another to said plural number of latch circuits includes:

15 a switch, receiving a plural number of clocks having respective different phases(referred to as multi-phase clocks), for selecting a plural number of sets of clock pairs from said multi-phase clocks; and

a plural number of interpolators, receiving plural sets of clock pairs, output from said switch, each interpolator outputting a signal the  
 20 delay time of which is prescribed by the time corresponding to interior division of a phase difference of said clock pair;

each of said interpolators including:

a circuit for turning a charging path and a discharging path of a capacitor on and off depending on logic values of input clock pairs; and

25 a buffer circuit for varying an output logic value when the  
magnitudes relation between the terminal voltage of said capacitor and a  
threshold value are inverted; the capacitance value of said capacitor being  
variably set by a control signal for determining the capacitance value;  
output signals of said plural interpolators being fed as clocks to said latch  
30 circuits; wherein

a circuit for controlling the phase of said clocks includes a decoder  
for decoding an output of said filter; and

switching of selection of said clock pairs in said switch is  
controlled based on an output signal of said decoder, with the interior  
35 division ratio of said plural interpolators being variably set and control  
being performed to advance or delay the phase of clocks supplied to said  
plural latch circuits.

2. The clock and data recovery circuits as defined in claim 1 further  
comprising

a selection circuit receiving all or part of outputs of said plural  
latch circuits to select outputs to be output as output data.

3. A clock and data recovery circuit comprising:

a switch receiving a plural number of clocks having respective  
different phases(referred to as multi-phase clocks), for outputting a plural  
number of sets of clock pairs therefrom;

5 a plural number of interpolators receiving a plural number of sets  
of clock pairs, output from said switch, for outputting signals the delay  
time of which is prescribed by the time corresponding to interior division  
of the phase difference of clocks of said clock pair;

a plural number of latch circuits for latching input data based on  
 10 output signals respectively output from said interpolators;

a counter circuit for increasing or decreasing an output value  
 based on output logic values of said plural latch circuits;

a filter for averaging an output of said counter circuit for a  
 predetermined time period;

15 a decoder for decoding an output of said filter; and

a selection circuit receiving a set of data output from said plural  
 latch circuits and clocks output from a preset one of said interpolators,  
 said selection circuit selecting data to be output to output the selected  
 data along with said clocks for varying a parallel number of the output  
 20 data and the clocks;

the switching of selection of clock pairs in said switch being  
 controlled based on an output signal from said decoder to variably set the  
 interior division ratio of said plural interpolators.

4. The clock and data recovery circuit as defined in claim 3 wherein said  
 counter circuit is made up of a charge pump circuit for charging and  
 discharging a capacitor with an upcounting signal and with a  
 downcounting signal, respectively, said upcounting signal and the  
 5 downcounting signal being first and second logic values of said output of  
 said latch circuit, an output voltage of said charge pump circuit being fed  
 to said filter.

5. The clock and data recovery circuit as defined in claim 3 wherein said  
 counter circuit is made up of an up/down counter and wherein a digital  
 output of said counting circuit is input to said filter of the digital filter

circuit.

6. A clock and data recovery circuit comprising:

a switch receiving a plural number of clocks having respective different phases(referred to as multi-phase clocks), for outputting a plural number of sets of clock pairs therefrom;

5 a phase shift circuit including a plural number of interpolators receiving a plural number of sets of clock pairs, output from said switch, for outputting output clocks the delay time of which is prescribed by the time corresponding to interior division of the phase difference of said received clock pair with a given control signal;

10 a plural number of flip-flops for sampling the input data with clocks output from said plural interpolators and for outputting the resulting sampled data;

a counter receiving a plural number of outputs of said flip-flops for upcounting or downcounting depending on the logic values of said outputs  
15 of said flip-flops;

a filter for time averaging a count output of said counter; and

a decoder for decoding an output of said filter;

said decoder outputting a switching signal for switching the combinations of the clock pairs in said switch, based on a decoded result  
20 of the output from said filter, said switching signal varying the interior division ratio in said plural interpolators; and

a selection circuit receiving plural sets of part or all of outputs of said plural flip-flops and clocks output from said first interpolator to render the parallel number of the output data and the clocks selectable.

7. The clock and data recovery circuit as defined in claim 6 wherein

the counter for counting outputs of said plural flip-flops is made up of a charge pump circuit for charging and discharging a capacitor with an upcounting signal and with a downcounting signal, respectively, said

5 upcounting signal and the downcounting signal being first and second logic values of said output of said latch circuit, respectively, and an output of said charge pump circuit is supplied to said filter.

8. The clock and data recovery circuit as defined in claim 6 wherein

said interpolator includes a circuit for turning a charging path and a discharging path of a capacitor on and off depending on the values of input clock pairs, and a buffer circuit for changing an output logic value  
5 when the magnitudes relation between the terminal voltage of said capacitor and a threshold value are inverted; the capacitance value of said capacitor being variably set by a control signal for determining the capacitance value.

9. The clock and data recovery circuit as defined in claim 6 wherein

each of said interpolators includes a logic circuit having first and second input terminals for receiving first and second input signals therefrom;

5 a switch inserted across a first power supply and an internal node and turned on when an output of said logic circuit is of a first logic value; and

a buffer circuit having its input terminal connected to said internal node and having an output logic value inverted on inversion of the  
10 magnitudes relation between said internal node voltage and a threshold

value;

there being also provided N pieces of second switches connected in parallel, each having one end connected to said internal node, and having a control terminal supplied with said first input signal from said first  
15 input terminal;

N pieces of third switches connected in parallel, each having one end connected to said internal node, and having a control terminal supplied with said second input signal from said second input terminal;

N pieces of fourth switches, connected in parallel across the other  
20 end of said second switch and a second power supply and each having a control terminal supplied with a control signal from said decoder so as to be turned on or off;

N pieces of fifth switches, connected in parallel across the other  
25 end of said third switch and the second power supply and each having a control terminal supplied with a control signal from said decoder so as to be turned on or off; and

a plural number of serial circuits inserted across said internal node and said second power supply and each being made up of a sixth switch and capacitor;

30 said sixth switch being turned on or off by a capacitance value determining control signal supplied to a control terminal of said sixth switch to variably control the capacitance value of the capacitor connected to said internal node.

10. The clock and data recovery circuit as defined in claim 6 wherein said decoder sets the interior division ratio of said interpolator

based on a time-averaged value of an output of said counter by said filter;  
and wherein

5           if the upper or lower setting value of said interpolator is reached,  
and it is still necessary to perform adjustment for further advancing or  
delaying the phase of the output signal of said interpolator, a switching  
signal for switching the clock pair combinations is provided to said switch  
adapted for selectively outputting clocks to be supplied to said  
10   interpolator.

11. The clock and data recovery circuit as defined in claim 6 wherein  
said multi-phase clocks are supplied from a voltage controlled  
oscillator of a phase locked loop (PLL).

12. The clock and data recovery circuit as defined in claim 6 wherein  
said multi-phase clocks are supplied from a multi-phase clock  
generating circuit; said multi-phase clock generating circuit including:

5           a frequency divider for frequency dividing an input clock to  
generate multi-phase clocks having respective different phases;

          a period detection circuit for detecting the period of said input  
clock; and

          one or plural number of multi-phase clock multiplexer circuits  
arranged in one or plural cascaded stages, receiving clocks of a plural  
10   number of phases (n phases) output by said frequency divider, and  
generating clocks obtained by a frequency multiplication of said received  
clocks;

          said multi-phase clock multiplexer circuits receiving n-phased  
clocks (first to number n clocks) comprising:

15         $2n$  pieces of timing difference division circuits outputting a signal corresponding to division of the timing difference of two inputs;

         odd-number timing difference division circuits (number  $(2I - 1)$  timing difference division circuit, where  $1 \leq I \leq n$ ), receiving the same clock being the number  $I$  among the  $n$ -phased clocks, as said two  
20    inputs;

         even-number timing difference division circuits (number  $2I$  timing difference division circuit, where  $1 \leq I \leq n$ ), receiving the number  $I$  and number  $(I+1)$  clocks among the  $n$ -phased clocks, where number  $(n+1)$  clock circulates to number 1 clock;

25         $2n$  pieces of pulse correction circuits; wherein the number  $J$  pulse correction circuit, where  $1 \leq J \leq 2n$ , receives as a first input an output of the number  $J$  timing difference division circuit, while receiving as a second input an output of the number  $((J+2) \bmod n)$  timing difference division circuit, where  $(J+2) \bmod n$  is a remainder obtained on dividing  
30     $(J+2)$  with  $n$ ; said number  $J$  pulse correction circuit outputting a NAND operation of said first input and a complemented signal of said second input;

$n$  pieces of multiplexing circuits, with the number  $K$  multiplexing circuit, where  $1 \leq K \leq n$ , receiving an output of the number  $K$  pulse  
35    correction circuit and with an output of the number  $(K+n)$  pulse correction circuit to output NAND thereof.

13.    The clock and data recovery circuit as defined in claim 12 wherein said timing difference division circuit includes:

         a logic circuit receiving signals from first and second input



terminals as inputs to output results of preset logical operation of said  
 5 first and second input signals;

a first switching device connected across said first power supply  
 and the internal node for receiving an output signal of said logic circuit  
 at a control terminal thereof;

a buffer circuit having its input terminal connected to said internal  
 10 node for switching a logic output value on switching of the magnitudes  
 relation between said internal node potential and a threshold value;

a second switching device connected across said internal node and  
 a second power supply and turned on or off based on the value of a signal  
 from said first input terminal; and

15 a third switching device connected across said internal node and the  
 second power supply and turned on or off based on the value of a signal  
 from said second input terminal;

there being a plural number of serial circuits each comprised of a  
 fourth switch and capacitor connected across said internal node and said  
 20 second power supply; said fourth switch device being controlled on or off  
 by the value of the period control signal supplied to a control terminal of  
 said fourth switch device to determine the value of the capacitance  
 connected to said internal node.

14. The clock and data recovery circuit as defined in claim 6 wherein

each of said interpolators includes a logic circuit having first and  
 second input terminals for receiving first and second input signals  
 therefrom;

5 a switch inserted across a first power supply and an internal node

and turned on when an output of said logic circuit is of a first logic value;  
and

a buffer circuit having its input terminal connected to said internal  
node and having an output logic value inverted on inversion of the  
10 magnitudes relation between said internal node voltage and a threshold  
value;

there being also provided N pieces of second switches connected in  
parallel, each having one end connected to said internal node, and having  
a control terminal supplied with a control signal from said decoder so as  
15 to be turned on or off;

N pieces of third switches connected in parallel, each having one  
end connected to said internal node, and having a control terminal  
supplied with a control signal from said decoder so as to be turned on or  
off;

20 N pieces of fourth switches, connected in parallel across the other  
end of said second switch and a second power supply and each having a  
control terminal supplied with said first input signal from said first input  
terminal;

N pieces of fifth switches, connected in parallel across the other  
25 end of said third switch and the second power supply and each having a  
control terminal supplied with said second input signal from said second  
input terminal; and

a plural number of serial circuits inserted across said internal node  
and said second power supply and each being made up of a sixth switch  
30 and capacitor;

said sixth switch being turned on or off by a capacitance value determining control signal supplied to a control terminal of said sixth switch to variably control the capacitance value of the capacitor connected to said internal node.

15. A clock control method for use in a clock and data recovery circuit including a plural number of latch circuits receiving input data in common; said latch circuits sampling the input data with transition edges of clock signals having phases shifted from one another, said clock  
5 signals supplied respectively to said latch circuits to output the sampled data;

a phase detection circuit for detecting a phase of a transition point of said input data associated with the clocks from outputs of said plural latch circuits and for outputting the detected phase;

10 a filter for smoothing an output of said phase detection circuit; and  
a circuit for controlling the phase of said clocks based on an output of said filter; said clock and data recovery method recovering the clocks and data based on the input data; comprising the steps of:

15 selecting by a switch receiving a plural number of clocks having  
respective different phases (termed multi-phase clocks), a plural number of sets of clock pairs from said multi-phase clocks and outputting the selected sets of the clock pairs;

20 with a plural number of interpolators receiving a plural number of sets of the clock pairs output from the switch, outputting a signal the delay time of which is prescribed by time corresponding to interior division of the phase difference of said paired clocks;

switching of selection of clock pairs in said switch being controlled based on an output signal of a decoder decoding the output of said filter; the interior division ratio of said interpolator being variably set to vary  
25 the phase of the clocks supplied to said plural latch circuits;

30 varying the capacitance value of each interpolator, having a circuit for turning a charging path and a discharge path of a capacitor on and off, depending on the logic value of the input clock pair, and a buffer circuit for changing an output logic value when the magnitudes relation between the terminal voltage of said capacitor and the threshold value is changed, by a set of switches being turned on and off with capacitance determining control signals to enlarge the frequency range that can be coped with.

16. The clock control method as defined in claim 15 wherein data that can be output as output data is made selectable from all or part of outputs of said plural latch circuits obtained on sampling said input data by the transition edges of phase shifted clocks.